LINE INTERFACE, MODE 2 (LI-2), 628055

GENERAL DESCRIPTION

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1. GENERAL

1.01 This Section provides a general description of the ITT D448 line interface, Mode 2 (LI-2), 628055, to the functional block diagram level.

1.02 Whenever this Section is reissued, the reasons for reissue will be listed in this paragraph.

1.03 The LI-2 multiplexes and demultiplexes the data from the two digroups of the D448 terminal, adds stuff bits and control bits, and interfaces the terminal to T1C line termination equipment. The unit makes the D448 end-to-end compatible with an M1C-type multiplexer.

2. DESCRIPTION

2.01 The unit mounts in the D448 multiplex shelf (common equipment mounting section) in connector J8C. Installation procedures for the unit are provided in Section ITTR-18-432.

2.02 The unit is available in Group -0 only.

2.03 The unit consists of three epoxy-glass printed circuit boards (PCBs), associated circuit components, and a front panel. The lower front edge of one PCB is fitted with a handle to facilitate insertion and removal of the unit from the shelf. An identification strip on the handle face indicates the unit mnemonic (LI-2), last three digits of the model number, last three digits of the part number, and issue letter. The unit mnemonic, part number, and issue letter are also located on the front panel.

2.04 The LINE ERRORS, NO PULSES, FRAME LOSS, LOCAL, REMOTE, PASS, and FAIL LEDs, the FAST TEST switch, and the LOOP test points are located on the front panel.

2.05 Printed circuit wiring is etched on both sides of each PCB. The PCBs are interconnected by 10-pin connectors. The unit inputs and outputs are terminated in gold-plated contacts on the rear edge of the right PCB. These contacts mate with a 70-pin contact edge connector on the rear of the multiplex shelf.

3. FUNCTIONAL OPERATION (FIG. 1)

TRANSMIT SIDE

A. 1.544-MHz Clock Generation and Control

3.01 Clock for the transmit side of the terminal can be generated by the clock selector and 1.544-MHz oscillator or provided by the office interface unit (OIU). When the $\overline{\text{SELECT}}$ lead from the OIU is set low, clock from the OIU on the TCL1544L lead is selected. When the $\overline{\text{SELECT}}$ lead is set high, the generated 1.544-MHz clock is selected.

3.02 The selected 1.544-MHz clock is sent to the Digroup A and B transmit logic units (TLUs) on the TCL1544A and TCL1544B leads, respectively. The clock is also sent to the elastic store and loop control circuit for timing purposes.

B. 3.152-MHz Clock Generation and Control

3.03 Clock for the transmit side of the LI-2 is generated by the crystal-controlled 3.152-MHz oscillator. The

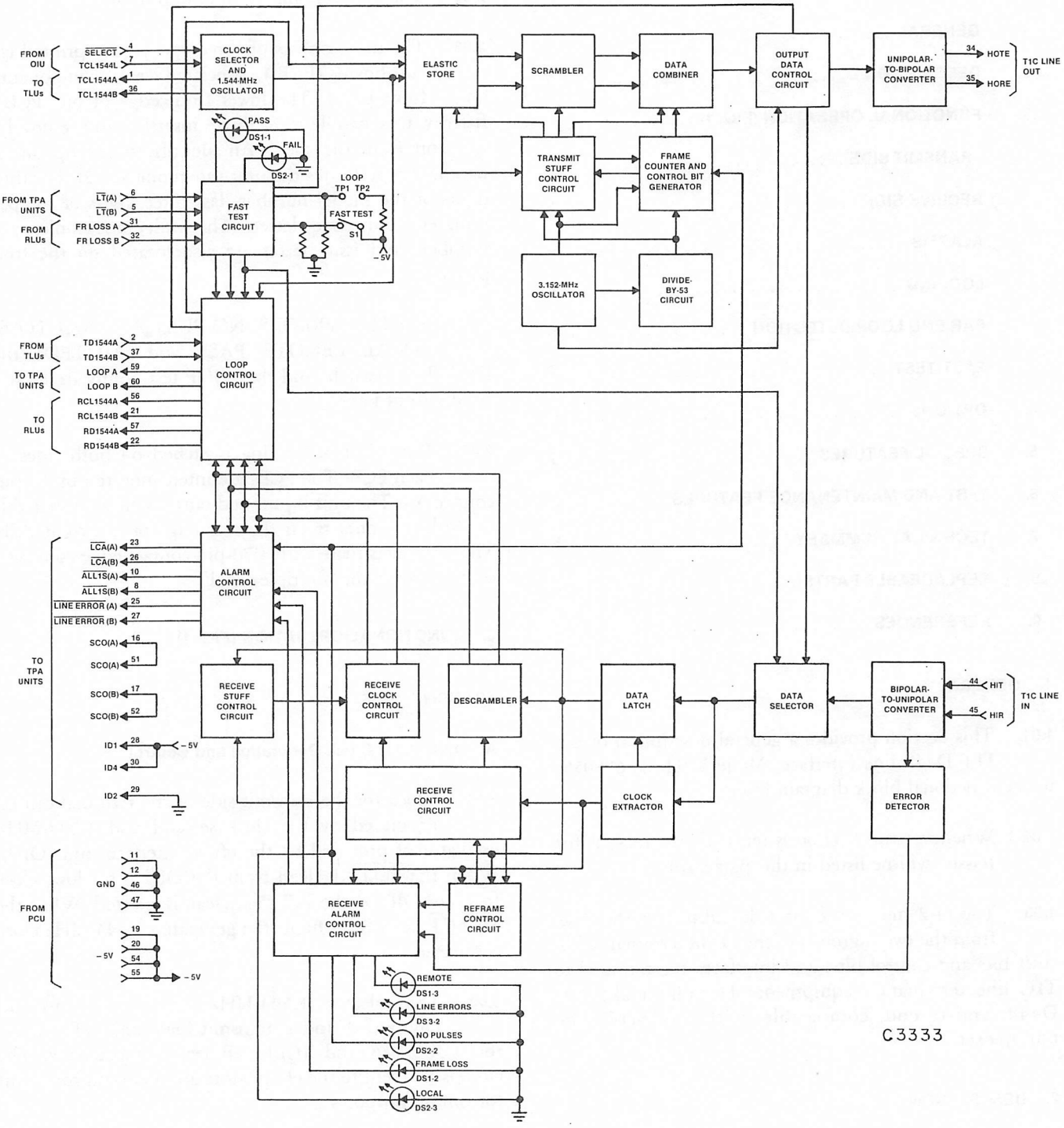

Fig. 1—LI-2, 628055, Functional Block Diagram

3.152-MHz clock is sent to the transmit stuff control circuit, the frame counter and control bit generator, the output data control circuit, and the divide-by-53 circuit.

3.04 The output of the divide-by-53 circuit is applied to the transmit stuff control circuit and the frame counter and control bit generator to identify the stuff bit time slots and the control bit (M, F, and C) time slots.

C. Data Transmission

3.05 The transmit bit stream from each digroup's TLU is applied to the loop control circuit on the TD1544A or TD1544B lead. During normal operation (no loop), the data is routed through the loop control circuit to the elastic store.

3.06 The elastic store reads in the data at 1.544 Mb/s and writes it into the scrambler at 1.546 Mb/s. Because data is being written out of the elastic store faster than it is being read in, the elastic store will eventually be depleted.

3.07 In order to prevent depletion of the elastic store, stuffing of the data is implemented. When the elastic store determines that it is nearing depletion, it sends a stuff request to the transmit stuff control circuit. The transmit stuff control circuit then signals the frame counter and control bit generator that stuffing is to take place.

3.08 The frame counter and control bit generator identifies the proper time slot for a stuff bit to the transmit stuff control circuit and sets the C (stuff) control bits to 111 for that frame. When the stuff bit time slot occurs, the transmit stuff control circuit inserts the stuff bit into the proper digroup bit stream in the scrambler and also inhibits the output of the elastic store for that bit stream for the time slot.

3.09 The output bit streams of the elastic store are applied to the scrambler. The scrambler performs scrambling on the data which is compatible with M1C-type scrambling. After scrambling, the two bit streams are applied to the data combiner.

3.10 The data combiner interleaves the bit streams from the two digroups bit-by-bit. This results in the formation of M1C-type words. One word consists of a bit from Digroup A and a bit from Digroup B. The data combiner also adds the control bits to the combined bit stream. The M, C, and F control bits are generated by the frame counter and control bit generator. These bits are combined with the data and stuff bits to form the complete M1C-type bit stream at 3.152 Mb/s.

3.11 Organization of the complete bit stream is as follows. A control frame consists of one control bit and 26 two-bit words. Six control frames make up one subframe. Within the subframe, control bits are generated in the following order: M, C, F, C, C, F. If a stuff bit is to be present, the C control bits are generated as 111. If no stuff is to take place, the C control bits are generated as 000. The framing (F) control bits follow the pattern 1010.

3.12 Four subframes make up one frame. Each subframe begins with an M control bit. Within the frame, the M control bits are generated in the order 011X. If a local alarm occurs (no pulse or frame loss), the receive alarm control circuit signals the frame counter and control bit generator to make the fourth M control bit a 0. This causes a remote alarm at the far end. If no local alarm exists, the fourth M control bit is transmitted as a 1.

3.13 The complete bit stream is sent to the output data control circuit. During normal operation (no loop), the output data control circuit passes the bit stream to the unipolar-to-bipolar converter.

3.14 The unipolar-to-bipolar converter provides a bipolar signal at ± 6V to the T1C line termination equipment on the HOTE and HORE leads.

RECEIVE SIDE

A. Clock Recovery

3.15 The clock extractor generates a 3.152-MHz clock signal from the incoming bit stream (via the bipolar-to-unipolar converter and data selector). The 3.152-MHz clock is distributed throughout the receive side of the LI-2 for timing purposes.

3.16 The 3.152-MHz clock applied to the receive control circuit is decoded to identify stuff bit time slots and control bit time slots. Additionally, the receive control circuit applies the clock signal to the receive clock control circuit.

3.17 The output of the receive clock control circuit is a 1.544-MHz clock signal which is applied to the receive side of the terminal on the RCL1544A and RCL1544B leads via the loop control circuit.

B. Data Transmission

3.18 Incoming data from the T1C line termination equipment is applied to the unit on the HIT and HIR leads. The data is converted to unipolar by the bipolar-to-unipolar converter and applied to the error detector (Para. 3.29) and the data selector.

3.19 During normal operation (no loop), the data selector passes the incoming bit stream to the clock extractor (Para. 3.15) and the data latch.

3.20 The data latch samples and latches the bit stream under control of the 3.152-MHz clock. The output of the data latch is sent to the descrambler, receive stuff control circuit, reframe control circuit, and receive alarm control circuit.

3.21 The descrambler separates the bit stream into the individual digroup bit streams and descrambles the bit streams. The receive control circuit identifies the locations of control bits and, during the occurrence of control bits, it inhibits the descrambler to prevent the control bits from entering the descrambler. The output of the descrambler is applied to the loop control circuit. The individual digroup bit streams are clocked out of the loop control circuit and sent to the appropriate receive logic unit (RLU) on the RD1544A or RD1544B lead.

3.22 The receive stuff control circuit identifies whether a stuff bit is present in either digroup's bit stream by examining the status of the stuff control bits. If two or more of the stuff control bits are 1, a stuff bit is present. The receive stuff control circuit then stops the clock to the appropriate digroup during the occurrence of the stuff bit to prevent the bit from being transmitted.

ALARMS

A. Local Alarms

Frame Loss Alarm

3.23 The reframe control circuit compares the framing code (1010) to the incoming bit stream M and F control bit time slots. When the two signals are aligned with each other, the receive side of the LI-2 is in frame and the system is functioning properly. When the reframe control circuit detects an out-of-frame condition, it signals the receive control circuit and the receive alarm control circuit.

3.24 The receive control circuit inhibits the receive timing to allow the framing code to slip back into synchronization with the incoming bit stream. This will require several slips to resynchronize the receiver.

3.25 The receive alarm control circuit turns on the FRAME LOSS and LOCAL LEDs. Additionally, it provides alarm signals to the alarm control circuit and the frame counter and control bit generator.

3.26 The signal to the frame counter and control bit generator causes the fourth M control bit to be set to 0, causing a remote alarm at the far end.

3.27 The signal to the alarm control circuit causes the $\overline{\text{LCA}}$(A) and $\overline{\text{LCA}}$(B) buses to the trunk processor and alarm (TPA) units to be activated. This causes digroup LCA alarms at the TPA units and the TPA units to initiate trunk processing.

No Pulses Alarm

3.28 The receive alarm control circuit continuously checks the status of the incoming data. If the incoming data is lost, the receive alarm control circuit turns on the NO PULSES and LOCAL LEDs and causes the events described in Para. 3.26 and 3.27 to occur.

Line Errors Alarm

3.29 The incoming bit stream applied to the error detector is monitored for bipolar violations. If such a violation occurs, the error detector signals the receive alarm control circuit. The receive alarm control circuit turns on the LINE ERRORS LED. However, neither digroup LCA alarms nor an LI-2 local alarm is caused by this condition.

3.30 The receive alarm control circuit also signals the alarm control circuit of the error condition. The alarm control circuit then notifies the TPA units of the condition on the $\overline{\text{LINE ERROR}}$(A) and $\overline{\text{LINE ERROR}}$(B) leads.

B. Remote Alarms

3.31 The receive alarm control circuit checks for the presence of a 0 in the fourth M control bit time slot. Such a condition signals the existence of a local alarm at the far end.

3.32 When the far end is in local alarm, the receive alarm control circuit turns on the REMOTE LED. This detection of a remote alarm does not directly cause digroup RMA alarms; however, the remote alarm detector circuitry in each RLU does detect the presence of a remote alarm via its digroup bit stream, thereby causing an RMA alarm at its TPA unit.

LOOPING

A. General

3.33 Two types of looping are incorporated in the LI-2. These are digroup looping and terminal looping.

B. Digroup Looping

3.34 Digroup looping occurs when the LOOP button on a digroup's TPA unit is pressed when the digroup

is in a carrier group alarm (CGA) condition. The loop signal is applied to the unit on either the $\overline{LT}$(A) or $\overline{LT}$(B) lead. The fast test circuit forwards the signal to the loop control circuit.

3.35 The loop control circuit then effectively ties that digroup's input bit stream (TD1544A or TD1544B) to its output (RD1544A or RD1544B).

3.36 This type of looping is used mainly during trouble location and allows the use of the fast test (Para. 3.46).

3.37 When a digroup is looped, the loop control circuit applies an all ones signal to the elastic store in place of the normal digroup bit stream. This all ones signal is transmitted to the far end to indicate near-end digroup looping.

3.38 The loop control circuit also signals the appropriate TPA unit on the LOOP A or LOOP B lead to turn on the TPA unit's LOOP LED.

C. Terminal Looping

3.39 Terminal looping (also called LI-looping) occurs when a shorting plug is inserted in the LOOP test points. This type of looping does not require the presence of a CGA condition.

3.40 The fast test circuit signals the output data control circuit. The output data control circuit then applies its normal output to the data selector. The data selector selects this data, also under control of the fast test circuit, as the receive data for processing by the receive side of the terminal.

3.41 The output data control circuit applies an all ones signal to the unipolar-to-bipolar converter in place of the normal bit stream. This all ones signal is transmitted to the far end to indicate near-end terminal looping.

3.42 The fast test circuit also signals the loop control circuit of the presence of terminal looping. The loop control circuit subsequently signals the TPA units on the LOOP A and LOOP B leads to turn on each TPA unit's LOOP LED.

FAR-END LOOP DETECTION

3.43 The receive alarm control circuit continuously checks the incoming bit stream for the presence of an all ones signal in either or both digroup's data.

3.44 When the far end is looped at only one digroup (or D bank), the receive alarm control circuit detects the presence of the all ones signal and notifies the alarm control circuit which signals the appropriate TPA unit on the $\overline{ALL1S}$(A) or $\overline{ALL1S}$(B) lead.

3.45 When the far-end terminal (or M1C-type multiplexer) is looped at its output, the receive alarm control circuit detects the presence of an all ones signal in both digroup's data and notifies the alarm control circuit which signals both TPA units on the $\overline{ALL1S}$(A) and $\overline{ALL1S}$(B) leads.

FAST TEST

3.46 As described in Para. 3.35, the digroup looping used during CGA conditions for trouble location causes a loop to occur at the front end of the LI-2. For this reason, the LI-2 could still be suspect if an alarm cleared when the digroup was looped. The fast test is therefore used to ascertain whether there is a fault in the LI-2 or the digroup's common equipment.

3.47 In order for the fast test to be used, only one digroup may be looped. When the FAST TEST switch is pressed, the fast test circuit causes the terminal to be looped for approximately 300 milliseconds. When, during this time, the FR LOSS A or FR LOSS B lead from the looped digroup's RLU is low, the PASS LED is turned on to indicate that the RLUs of both digroups are synchronizing to their respective TLU's data while the data is being multiplexed and demultiplexed by the LI-2. This indicates that no fault exists in the LI-2.

3.48 When the FAIL LED is turned on, the opposite of the above is true. This indicates that the LI-2 is faulty.

3.49 During the fast test, the $\overline{LCA}$(A) and $\overline{LCA}$(B) buses to the TPA units are activated by the alarm control circuit to cause digroup LCA alarms.

4. OPTIONS

4.01 This unit has no field-selectable options.

5. SPECIAL FEATURES

5.01 If the LI-2 is removed from the multiplex shelf while the terminal is in service, digroup LCA alarms will occur. The SCO loops on the unit are fed to the TPA unit. If a loop opens, the TPA unit causes a local alarm.

6. TEST AND MAINTENANCE FEATURES

6.01 A description of the test and maintenance features of the unit is provided in Table A.

TABLE A

FEATURE	REF. DES.	FUNCTION
PASS LED (green)	DS1-1	Indicates that RLUs of both digroups are synchronizing to TLUs data while data is being multiplexed and demultiplexed by LI-2; can be activated only when terminal is looped and FAST TEST switch on LI-2 is pressed; will remain on until digroup is unlooped.
FRAME LOSS LED (red)	DS1-2	Indicates failure to synchronize to incoming data on T1C line by LI-2 demultiplexer.
REMOTE LED (red)	DS1-3	Indicates that far-end multiplexer or far-end LI-2 is experiencing local alarm and sending remote alarm code to near-end LI-2.
FAIL LED (red)	DS2-1	Indicates that conditions described for PASS LED above are not true; can be activated only as described above; will remain on until digroup is unlooped.
NO PULSES LED (red)	DS2-2	Indicates that no data being received by LI-2 from incoming T1C line.
LOCAL LED (red)	DS2-3	Indicates that either frame loss or no pulses indication present at LI-2.
LINE ERRORS LED (red)	DS3-2	Indicates bipolar violations being received from incoming T1C line; cannot be turned on during looped conditions.
FAST TEST Switch	S1	Indicates fast test when pressed and one digroup (only) is looped.
LOOP Test Points	TP1 and TP2	Provides a means of looping the terminal when terminal is not in trunk processing (used for installation only).

6.02 The looping initiated at the TPA unit requires that the terminal be in a CGA condition, and while looped the CGA condition cannot be cleared. The alternate looping method provided by the LOOP test points is called the LI- loop. This LI- loop, initiated by the insertion of a shorting plug in the LOOP test points, does not necessitate a CGA condition as opposed to the terminal looping. The intent of the LI- loop is to provide for "hot-standby" operation between system installation and final system turn-up, should that be an extended period of time. During LI- loop, the alarm reporting is active and all channel unit signaling highways are available for testing purposes.

7. TECHNICAL SUMMARY

7.01 A summary of technical specifications for the unit is given in Table B.

TABLE B

ITEM	SPECIFICATION
DC POWER	
Voltage	−5.0 ±0.25 Vdc
Current	858 mA maximum, 465 mA nominal
T1C LINE OUTPUT	
Line Rate	3.152 Mb/s ±30 ppm
Line Code	Bipolar
Output Impedance	110 ohms nominal
Pulse Characteristics	
Base-to-Peak Height	±6.0 ±0.6V
Width	160 ±20 ns
Maximum Rise and Fall Time	20 ns, 10 to 90% of pulse height

TABLE B (CONT)

ITEM	SPECIFICATION
T1C LINE INPUT	
Line Rate	3.152 Mb/s ± 30 ppm
Line Code	Bipolar
Input Impedance	100 ohms nominal
Pulse Characteristics	
Width	130 ns minimum
Base-to-Peak Height	± 1.5V minimum
OPERATING ENVIRONMENT	
Temperature	0° to 55°C
Humidity	To 95% at 40°C (no condensation)
Altitude	To 14,000 ft (4,267 m)
DIMENSIONS	
Height	5.0 in. (12.7 cm)
Width	2.4 in. (6.1 cm)
Depth	9.6 in. (24.4 cm)
WEIGHT	1.0 lb (0.5 kg)

8. REPLACEABLE PARTS

8.01 This unit has no field-replaceable parts.

9. REFERENCES

9.01 The engineering drawings noted in Table C were used in the preparation of this Section.

TABLE C

TYPE	DRAWING NO.
Assembly	628055-000
Schematic	628055-002

9.02 Related information on the LI-2 may be found in the ITTR Sections referenced in Table D.

TABLE D

TITLE	SECTION NO.
Connectorized Multiplex Shelf, (MS/WC7, MS/WC5, MS/C7 and MS/C6), 628001, 628005, 628011 and 628015 — General Description	ITTR-18-005
Mode 2 Common Equipment — Installation and Pretest	ITTR-18-432